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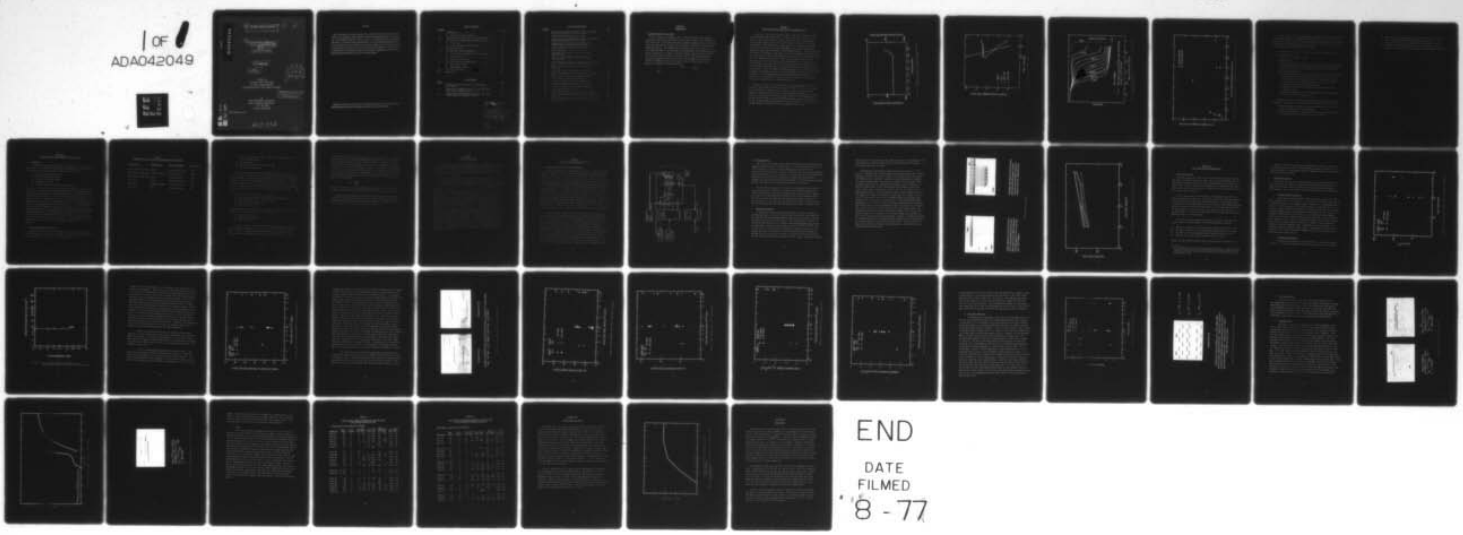

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NEW MEMORY DEVICE STRUCTURES

Interim Technical Report No. 2

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by

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INTRODUCTION

A. Program Objective and Goals

The Air Force has requirements for a radiation-hardened shift register analog memory device for applications such as data storage, data re-formatting, and signal delay. The device must have low power consumption and a wide dynamic range, but nonvolatility is not required because of the nature of the real-time system application. The objective of the program carried out under Contract No. F33615-74-C-1054 is to investigate new semiconductor analog memory structures having the potential for extreme radiation hardness. Device performance goals are (1) sample rate of 10 MHz, (2) dynamic range of 10^3, (3) maximum power dissipation of 40 microwatts per bit, (4) total dose hardness to ionizing radiation of 10^6 rad (Si), and (5) recovery within 10 milliseconds after exposure to a pulse of ionizing radiation.

SECTION II

ADDITIONAL RESULTS FROM THE FIRST RADIATION TESTS

Since the first interim technical report, additional measurements and evaluations have been made on the test samples from the first total dose test. Figure 1 shows a plot of charge transfer efficiency versus frequency for a typical buried channel device after irradiation to a level of 3×10^6 rad. The response is flat below about 12 MHz, just as it was before irradiation. It should be noted again here that the 99.95% CTE of these buried channel samples was much lower than typical buried channel devices. Figure 2 illustrates the change in threshold voltage versus total dose for MOSFETs having different gate oxide types as shown. The magnitude of these shifts is much smaller than the high frequency MOS capacitor flatband shifts reported earlier, which ranged up to 65 volts for devices on the same samples. The explanation for this difference is illustrated in Figure 3, which shows that the CV curve of surface channel capacitors shifts with frequency for devices with high surface state density. Since the MOSFET threshold measurements were made at a near-zero frequency, the measured V_T shifts should be compared to the low frequency flatband shifts. This large dependence of flatband voltage on frequency is indicative of a high surface state density after irradiation, as was shown by the greatly reduced CTE of the surface channel CCDs.

Figure 4 indicates the relative increase in leakage current for surface and buried channel CCDs irradiated at doses of 10^5 to 3×10^6 rad. The cause of the difference in leakage increase between surface and buried channel samples is not known due to pre-irradiation measurements problems, but it may be due to a large density of surface states and hence surface leakage for the surface channel devices. The pre-irradiation leakage currents for both the CCD and the gated diode were characterized more completely for the second group of test samples, as discussed in the next section of this report.

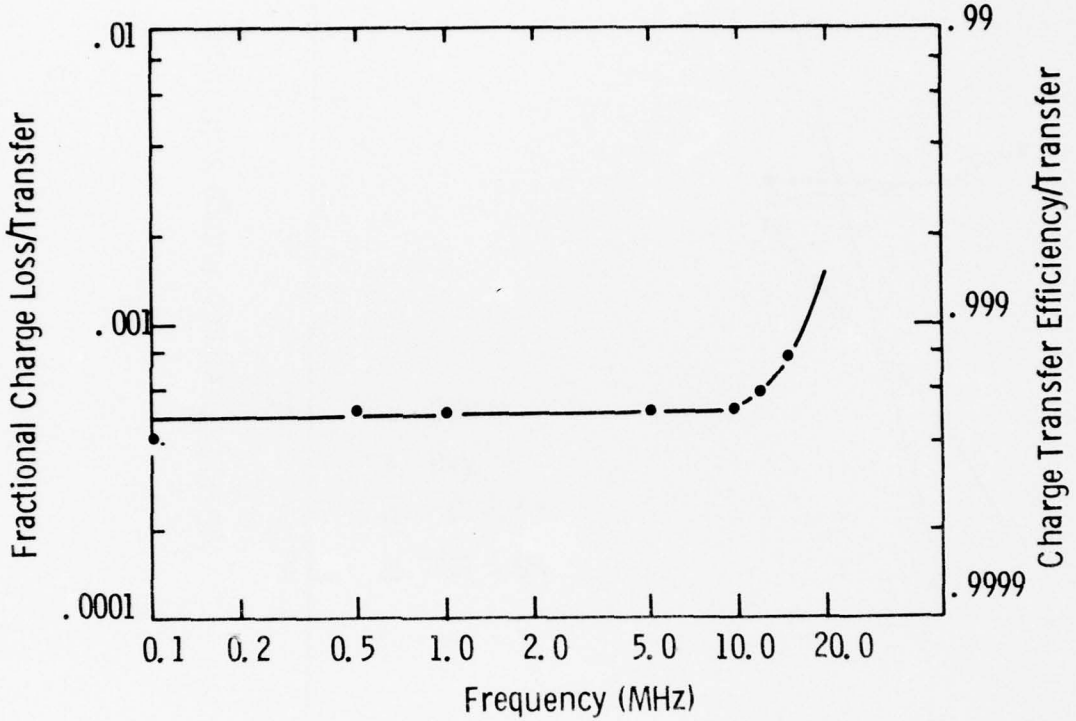


Figure 1 Variation of CTE with Frequency for Buried Channel CCD after Total Dose of 3×10^6 Rad (Si)

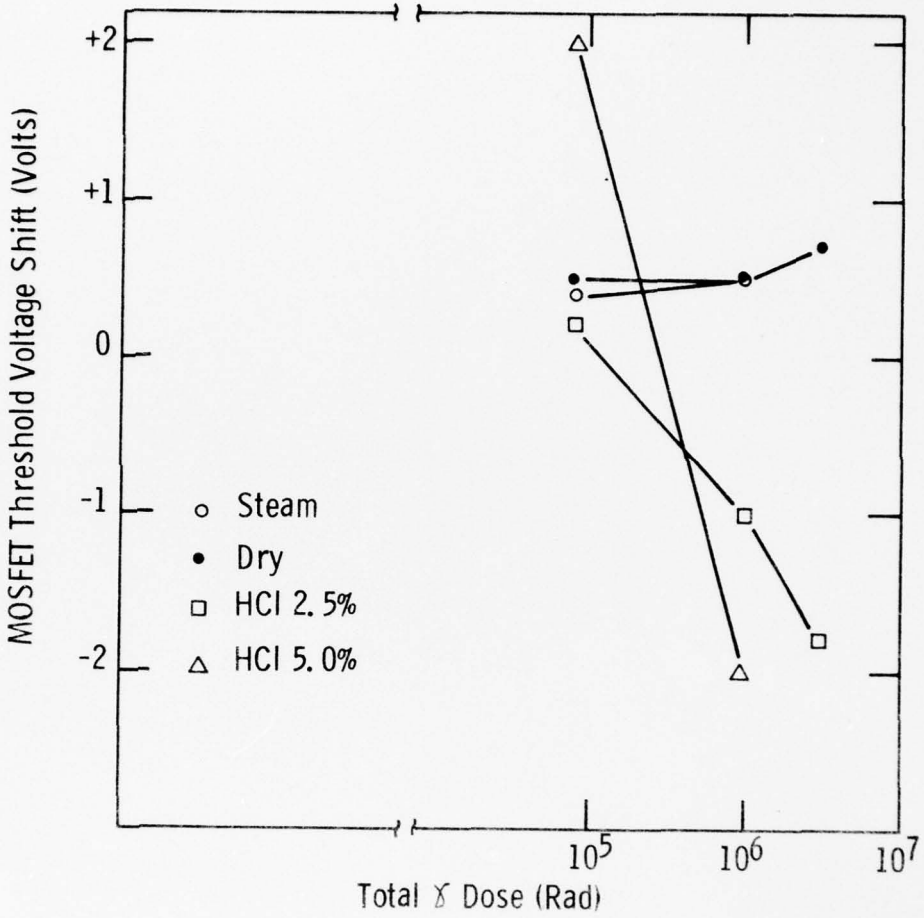


Figure 2 Surface Channel MOSFET Threshold Variation with γ Dose

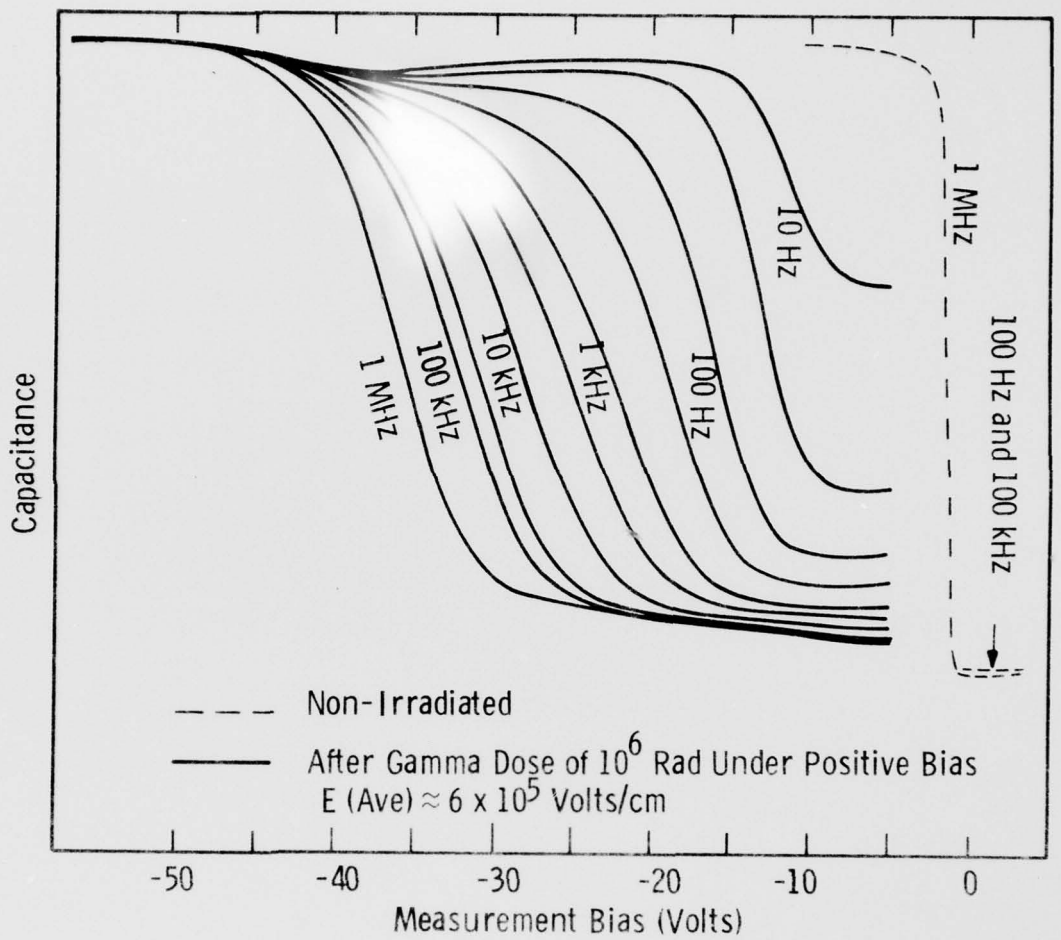


Figure 3 Curves Showing CV Shift Versus Frequency for Surface Channel MOS Capacitors with HCℓ Oxide

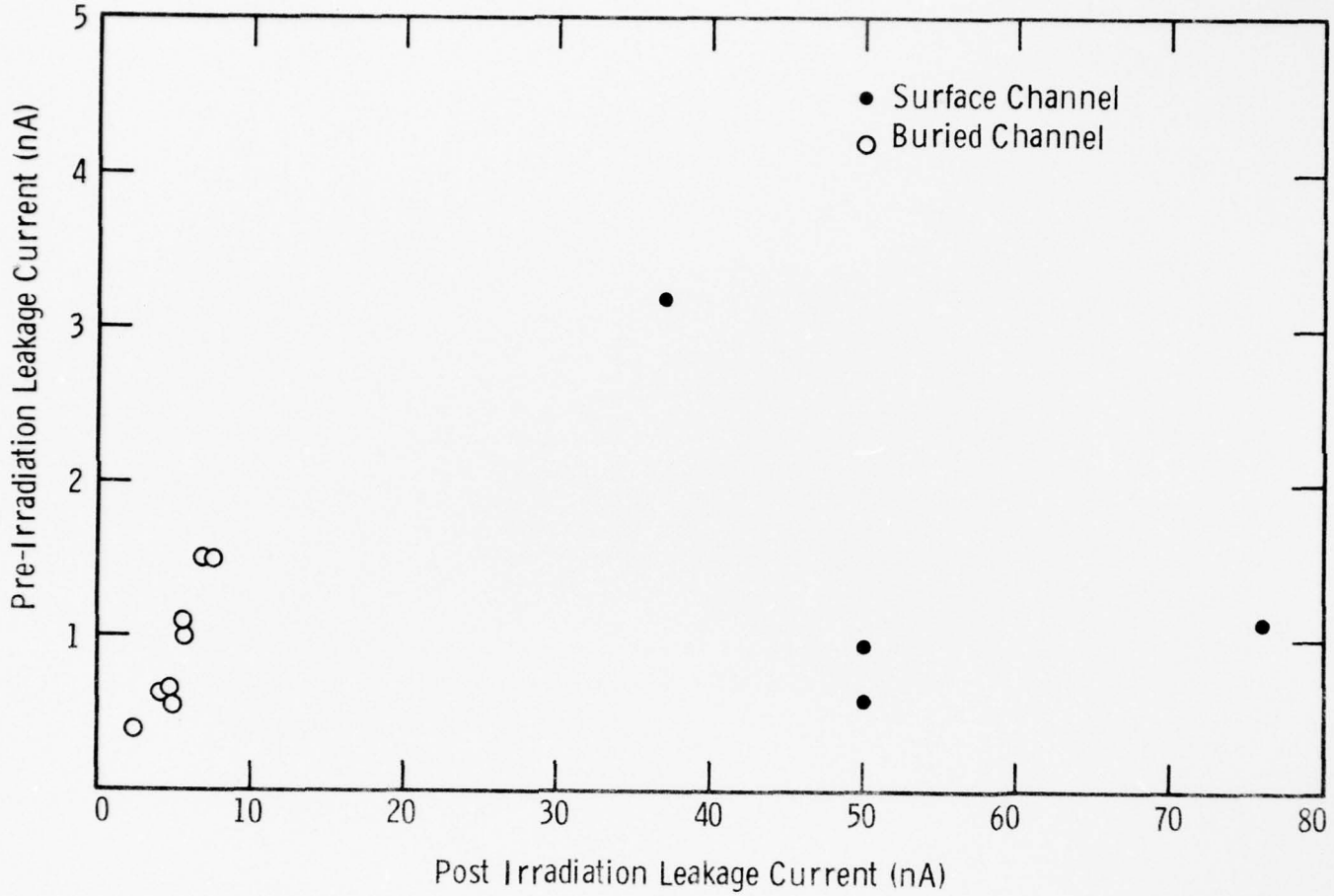


Figure 4 Leakage Current Increase With γ Radiation for Surface Channel and Buried Channel CCDs

The CCD output noise after irradiation was measured for the buried channel devices from this test. The output noise was found to be dominated by the shot noise on the leakage current. This is as would be expected, since these samples typically had dark leakage currents of the order of 1000 nA/cm^2 after irradiation (as opposed to $\approx$ 100 nA/cm^2 before irradiation).

The following is a summary of results from the first radiation tests:

- Surface state buildup
  - N_{ss} of up to 10^{12} per eV/cm^2
- Oxide hardness
  - HCℓ grown oxides have large CV shifts due to interface state buildup
  - 950° steam and 1100° dry oxides are equal when used with e-beam metal
  - Diffused chrome is not effective when used with HCℓ grown oxide
- CCD total dose hardness
  - Surface channel devices not usable at 10^5 rad due to CTE degradation
  - Buried channel devices had no loss of CTE at 3×10^6 rad; input level shift of ≈ 4 volts, due to V_T shift; reduced G_M of MOSFETs
  - Typical dark current leakage increase of five times for buried channel and > 50 times for surface channel
  - Implanted and epitaxial layer buried channel CCDs exhibited similar hardness
  - Dominant noise source in buried channel devices tested appeared to be shot noise on leakage current.

Conclusions drawn from these results which were used in selecting the fabrication processes for the second group of test samples are listed below.

- HCℓ grown oxides show poorer radiation hardness than dry or steam oxide; therefore, use dry or steam oxide.
- Buried channel hardness is much greater than surface channel hardness for total dose effects; therefore, use buried channel.

- Epitaxial layer buried channel devices are not harder than implanted layer devices; therefore, use ion implanted buried channel, since control of the doping and placement of the buried layer is easier.
- Buried channel CCD hardness is determined by input/output devices; therefore, use oxide hardening techniques to improve MOSFET hardness.

SECTION III
DEVICES FOR THE SECOND GROUP OF RADIATION TESTS

A. Processing

On the basis of conclusions drawn from the results of the first total dose tests, it was decided to include the following process variations in the fabrication of devices for the second group of radiation tests:

(1) dry and steam grown gate oxides,
(2) diffused chrome-doped oxide,
(3) implanted chrome-doped oxide,
(4) nondoped oxide, and
(5) thermally evaporated and e-beam evaporated metal.

Since it was impractical to test all possible combinations of these process variations, the most promising ones were chosen. Continued problems with the source for chrome implantation prevented inclusion of ion implanted oxides. The main processing features of the slices from which the test samples came are listed in Table I. Althouth HCℓ was used to clean the furnace tubes prior to gate oxide growth, no HCℓ was introduced during growth. The n-type layer for buried channel operation was formed by implanting $1.7 \times 10^{12}/cm^2$ phosphorus ions at an energy of 190 kEV, followed by a 60 minute 1100°C drive in N_2. A PSG stabilization layer was formed at 900°C, and a deposited nitride overcoat layer was applied over the metallization for mechanical damage protection. The metallization is the double-level aluminum system using anodic aluminum oxide for interlevel insulation, which provides a sealed coplanar overlapping gate structure as described in Interim Technical Report No. 1 for this contract.

B. Pre-Irradiation Characterization

The CCD chips used for the test samples are of the same design used in the first group of tests and were described in Interim Technical Report No. 1. The test devices available in each of these samples are:

TABLE I

PROCESS VARIATIONS OF SLICES FOR SECOND GROUP TEST SAMPLES

Oxide Growth	Oxide Doping	Metal Deposition	Lot-Slice No.
950°C Steam (Dry-Wet-Dry)	None	Thermally Evaporated	68-1
950°C Steam (Dry-Wet-Dry)	Diffused Chrome	e-Beam Evaporated	68-2,3
950°C Steam (Dry-Wet-Dry)	None	e-Beam Evaporated	68-4,9
1000°C Dry	None	Thermally Evaporated	68-6,7
1000°C Dry	Diffused Chrome	e-Beam Evaporated	68-8
1000°C Dry	None	e-beam Evaporated	68-5

(1) 150-bit, four-phase CCD shift register with floating diffusion/ source follower output,
(2) MOS gated diode,
(3) short channel MOSFET with W/L of 10, and
(4) MOS gate oxide capacitor.

The 28 test samples were carefully characterized before irradiation. The performance parameters of the buried channel CCDs in this group of samples were outstanding. Typical charge transfer efficiencies were from 0.99992 to 0.99998 at 1 MHz. Dark leakage currents typically were from 3 to 10 nA/cm^2 at clock voltages of 15 volts. Because the dark currents were so low and these were buried channel devices, the dominant noise source was the noise generated by the output source-follower. The following measurements were made on a 100% basis:

(1) charge transfer efficiency without fat zero,
(2) CCD integrated leakage current pattern and average leakage,
(3) CCD total noise and source follower noise,
(4) MOSFET threshold voltage, and
(5) gated diode CV curves.

Since the parameters listed below were relatively constant for devices from the same slice, they were measured on a sample basis.

(1) source follower gain,
(2) CTE versus frequency, and
(3) full well capacity.

The charge transfer efficiency with and without fat zero was measured on several devices and was found to be the same within the accuracy of measurement. This is as expected on buried channel devices with such low bulk state densities as indicated by the low dark leakage currents. To eliminate

the effects of leakage in the output circuit and to show spatial variations in the leakage currents, integrated leakage measurements were made by stopping the clocks with one phase high for a period of time and collecting leakage current charge. After an integration time sufficient to collect a measurable fraction of a full well, the charge was clocked to the output, and a photograph was made of the output waveform. The voltage, v, corresponding to a given CCD bit is related to the leakage current density, J_L, in the vicinity of that bit by the following relationship if the shift out time is negligible compared to the time of integration.

$$J_L = \frac{C_N v}{T S_B A_v} \quad ,$$

where C_N is the total capacitance of the output diffusion, A_v is the source-follower voltage gain, T is the integration period, and S_B is the bit area.

The CCD noise was measured using the low noise input technique described in the first interim technical report and a correlated double-sampling scheme to eliminate output "kTC" noise. Under these conditions, the dominant noise source typically was found to be the output amplifier circuit.

SECTION IV
RADIATION TEST PLAN

The radiation tests for the second group of test samples were to include tests of both total dose effects and high dose rate pulse effects of ionizing radiation. It was decided to test one sample (containing four different devices) from each of the six process variations listed in Table I in each of the four tests listed below.

(1) High dose rate pulse (γ) recovery tests (20 MeV electrons).
(2) Total dose gamma ray test using Co^{60} (1.2 MeV) source at 10^6 rad level.
(3) Total dose gamma ray test using Co^{60} (1.2 MeV) source at 10^7 rad level.
(4) Total dose tests at levels from 0 to 10^6 rad using 20 MeV electrons.

This test plan required the fabrication, testing, and characterization of 24 buried channel test samples plus spares and units for use in setting up the dose rate tests. After completion of the dose rate tests (Test No. 1), which exposed the samples to a total of only about 10^4 rad, the devices were not noticeably degraded; therefore, it was decided to use these samples in an additional 10^6 rad total dose Co^{60} test, but at a reduced clock voltage of 8 volts, as was used in the first group tests. It had been decided to use a clock voltage of 12 volts in the total Co^{60} gamma dose tests (Nos. 2 and 3 above), since these samples could be operated buried channel with clocks up to 15 volts. Operation at these higher clock levels may be desirable in some applications because the full well capacity and, hence, the dynamic range, is increased, although the clock drive power is also increased. While at the test facility, it was decided to test two of the unused buried channel spare samples at a total dose gamma level of 3×10^5 to give data at an additional level. Two surface samples were also prepared for a 1.2 MeV Co^{60} total dose gamma test at 10^4 rad.

SECTION V
HIGH DOSE RATE PULSE RECOVERY TEST

A. Description of Equipment and Test Procedure

Charge coupled devices are generally very efficient collectors of photo-generated carriers, a property which makes them useful as imagers. However, this same property makes them subject to interrupted operation, and even possible burnout, when exposed to high dose rate bursts of ionizing radiation. Excessively high currents can flow causing burnout (metallization and junction thermal damages) when a large amount of photo-generated charge is collected by a reverse bias diffusion such as the drain of the output reset or source-follower MOSFETs in the CCD output circuit. These diffusions are usually connected directly to a power supply so that the currents are limited only by circuit metallization and contact resistance. However, in many cases, it is possible to insert a small resistance of the order of 100 ohms to help limit peak currents without appreciably degrading circuit performance. The purpose of this test was to determine the time required for the device to recover to normal operation after saturation from a flood of photocurrent caused by burst of ionizing radiation. Burnout effects at high dose rates were also monitored.

To measure circuit recovery time, the CCD must be operated at normal voltage levels and the output monitored during and after the radiation pulse. This, in turn, requires that all the clock generator and driver electronics must be sufficiently hardened and/or shielded, or that they must be located outside of the radiation chamber and drive the CCD through long cables. The latter approach was used for these tests. High speed 50 Ω cable driver integrated circuits were used to drive the four clock phases and the precharge gate, as shown in Figure 5. Another of the same circuits was placed behind a 5 cm thick aluminum shield to serve as an output cable driver for the CCD output. This device was mounted in a socket so it could be easily replaced if it became too degraded after being used for many radiation tests. However, the cable driver IC survived all the radiation tests without apparent damage.

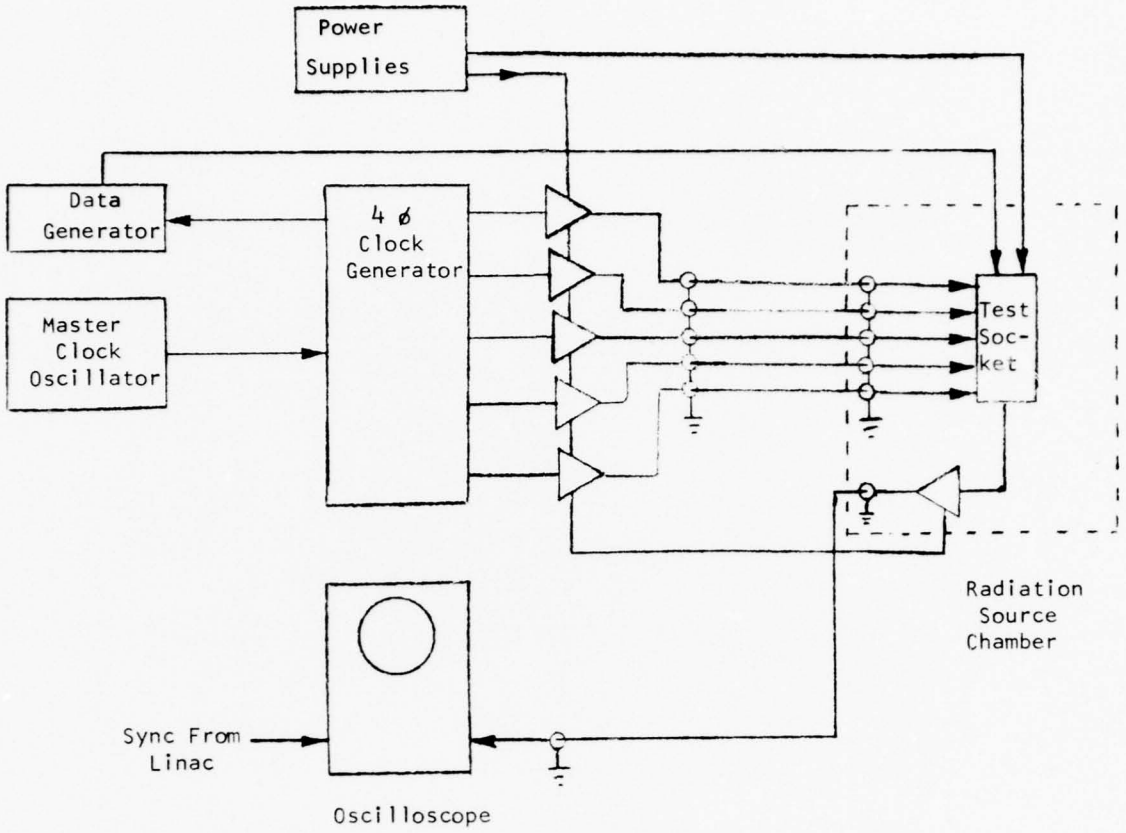


Figure 5 Dose Rate Recovery Test Set Block Diagram

B. Source Facility

The Linac at the Nuclear Weapons Effects Laboratory at White Sands Missile Range was selected as the $\dot{\gamma}$ radiation source. It can give dose rates of up to 10^{11} rad/second in the direct electron beam mode with pulse widths of from 50 nsec to several μsec; and pulse repetition rates up to 10 pulses/second. Flash x-ray machines such as the Hermes II at Sandia Labs can give Bremstrahlung mode dose rates of up to 10^{12} rad/second, but would have been much more expensive to use and would have taken much longer for the planned tests because of their much slower pulse rate of only one pulse in 20 minutes.

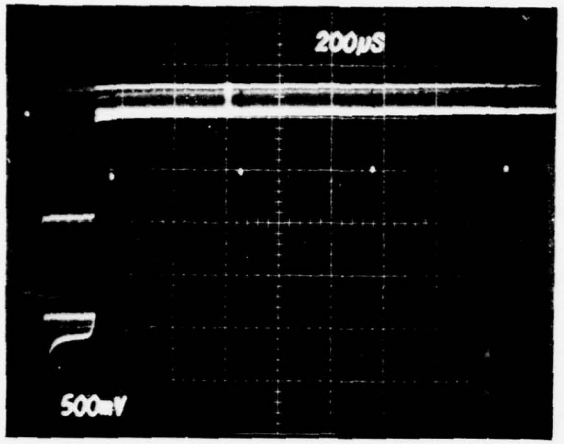
The electron beam output energy level was approximately 20 MeV, and the pulse width was set at 100 nsec. The dose rate was measured by means of a silicon diode that was calibrated by measuring the total dose from a number of pulses with a thermoluminescent dosimeter using lithium fluoride pellets. The dose per pulse was divided by the measured pulse width to obtain the average dose rate. The dose rate was varied by moving the test fixture away from the Linac output window along the beam axis by means of a movable table.

C. Experimental Results

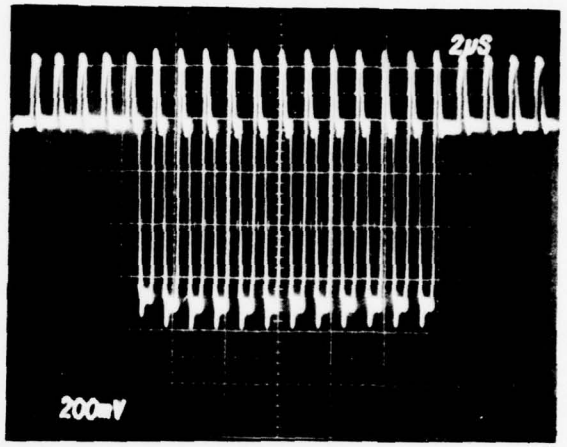
A trigger pulse from the Linac control system was used to trigger the oscilloscope sweep at the time of the electron pulse so that the output waveform from the CCD could be photographed during and after the pulse. The CCD was operating at normal bias level with a 1 MHz clock rate and a repetitive electrical input pulse to permit recovery time and performance after recovery to be recorded. Tests were made at dose rate levels of 10^8, 10^9, 10^{10}, and 4×10^{10} rad/sec. Each device was successively tested at these rates. The maximum dose rate was limited to 4×10^{10} rad/sec because the thickness of the shield on the test fixture to protect the output cable driver prevented the test sample from being closer than 5 cm to the window. The output waveforms

from the test of a typical device are shown in Figure 6. The responses of all the devices were very much alike, as can be seen by the plot of recovery times versus dose rate in Figure 7.

The photocurrent generated by a radiation pulse is given by $I_p = \dot{Y}gV$ where $\dot{Y}$ is the dose rate, g is the photocurrent generation rate for the device material ($g = 6.4 \times 10^{-6}$ A/(cm^3 - rad/sec) for silicon) and V is the volume over which charge is collected. The rate at which charge can be clocked out of the CCD is proportional to the full well capacity and clock rate (after the normal bias levels are regained in the output circuit). Therefore, it should be expected that similar results would be obtained for thest test samples because they all had similar volumes and full well capacities and the same clock rates. It can be seen from Figure 6 that for pulse levels to 10^{10} rad/sec the recovery was complete in about 250 μsec. However, for the 4×10^{10} rad/sec level there was an increased leakage current output that decayed with a time constant of about 500 μsec. The reverse-biased leakage characteristics of the input diode and reset and source-follower transistors were found to have a resistive component of about 5 kΩ after this irradiation test. Other diodes on the sample that were not reverse-biased from a low impedance source did not exhibit this type of leakage. This indicates that the devices were at the beginning of the thermal damage range (burnout) at the 4×10^{10} rad/sec rate for 100 nsec pulses. However, it should be possible to increase the level of the onset of thermal damage by use of a small amount of series resistance in series with the supply leads. This was not done in these tests, since the evidence of thermal damage was not found until some time after the tests were made.



Output waveforms of buried channel CCD showing operation during and after exposure to a 100ns wide pulse of 20 Mev electrons from Linac dose rate is 10^{10} Rad/sec.



Expanded scale waveform of CCD signal pulse demonstrating good CTE after recovery from saturation caused by photocurrent from radiation pulse.

Figure 6 Output Waveforms

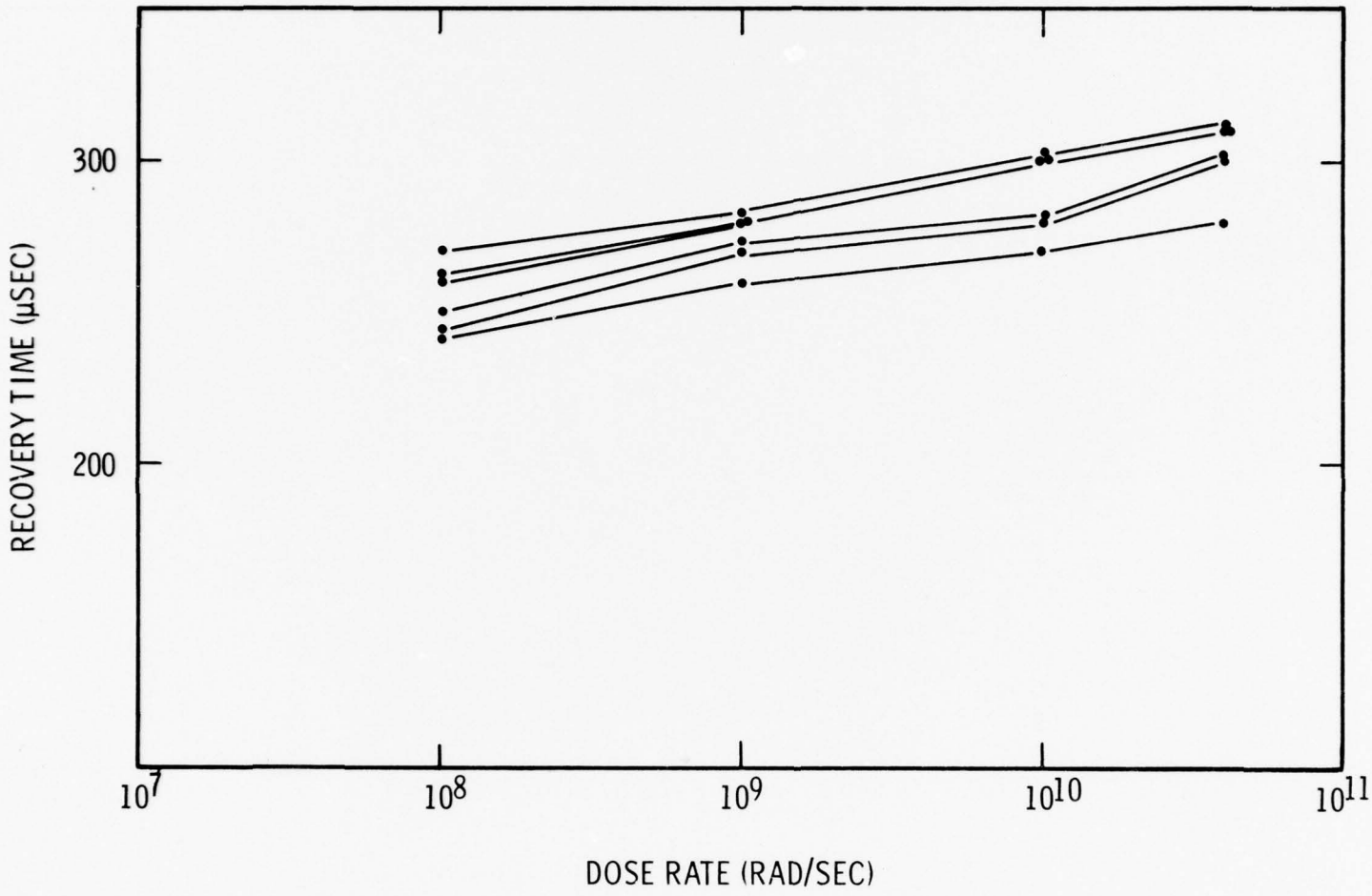


Figure 7 CCD Recovery Time after 100 nsec Linac 20 MeV Electron Pulse

SECTION VI
THE SECOND TOTAL DOSE GAMMA TESTS

A. Description of Test

Total dose gamma tests (Tests 2 and 3) were made on test samples at the same time the dose rate tests were made. The source used for these tests was the Co^{60} Gamma Radiation Facility at the Nuclear Weapon Effects Laboratory at White Sands. The test fixture and bias conditions for these tests were the same as those used for the first test,* except that a clock voltage of 12 volts was used for part of the tests.

The CCD input diode and precharge drain and the gated diode diffusion were reverse-biased to +24 volts. The source and drain of the output source-follower and the test MOSFET were connected to ground, as was the substrate. It has been found that grounding the source and drain of these MOSFETs produces unrealistic oxide bias conditions and results in much larger threshold shifts and gain degradation than occur under normal operating conditions in the source-follower. In future tests these points will be either biased to normal operating levels or reverse-biased.

A 50% duty cycle clock pulse was applied to all gates. The test dose levels, number of devices tested, and clock voltages were as follows:

- 10^6 rads - (Test No. 2) six buried channel samples with 12 volt clock.
- 10^7 rads - (Test No. 3) six buried channel samples with 12 volt clock.
- 3×10^5 rads - two buried channel spare samples with 8 volt clock.
- 10^6 rads - six buried channel samples with 8 volt clock.

(These were the samples previously used in the dose rate test (Test No. 1).

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* It was incorrectly stated in Interim Technical Report No. 1 that the source and drain of the output source-follower and test transistor were also connected to +24 volts. The correct conditions for the first group of tests are those given here.

The test units were irradiated to the desired dose level at a dose rate of 0.5×10^6 rad per hour or less. Dose rates were measured by means of lithium fluoride dosimetry, and the samples were then exposed at that rate for the time required for the desired dose.

B. Experimental Results

The samples from the total dose tests were first tested approximately five days after exposure. However, no short-term self-annealing was seen on the electron beam irradiated devices that were monitored during and immediately after exposure, so it is not likely that such effects occurred in these devices.

1. Charge Transfer Efficiency

The change in charge transfer inefficiency (CTI) with dose for Co^{60} gamma radiation is shown in Figure 8. It can be seen that there is wide variation in the CTE degradation from sample to sample. However, it is encouraging that for four of the nine samples at 10^6 rad the change in CTI was 10^{-4} or less. It should also be noted that all zero-dose CTE values are without fat zero, but the increased leakage current levels provided an unavoidable fat zero in the post-irradiation measurement on many devices. As mentioned above, these leakage currents can be greatly reduced on some devices by going to a positive substrate bias. However, in some cases, at the optimum substrate bias for reducing leakage current, the charge transfer efficiency is reduced. Figure 9 shows the variation of CTE with frequency after irradiation for a typical device. No measurable frequency response change is seen. Low frequency measurements after irradiation are limited by increased leakage currents to clock rates of about 25 kHz and above on some samples.

2. Threshold Voltage Shifts

The threshold voltage shifts for the MOSFET test transistor are shown in Figure 10. These shifts were more than ten times larger than the threshold

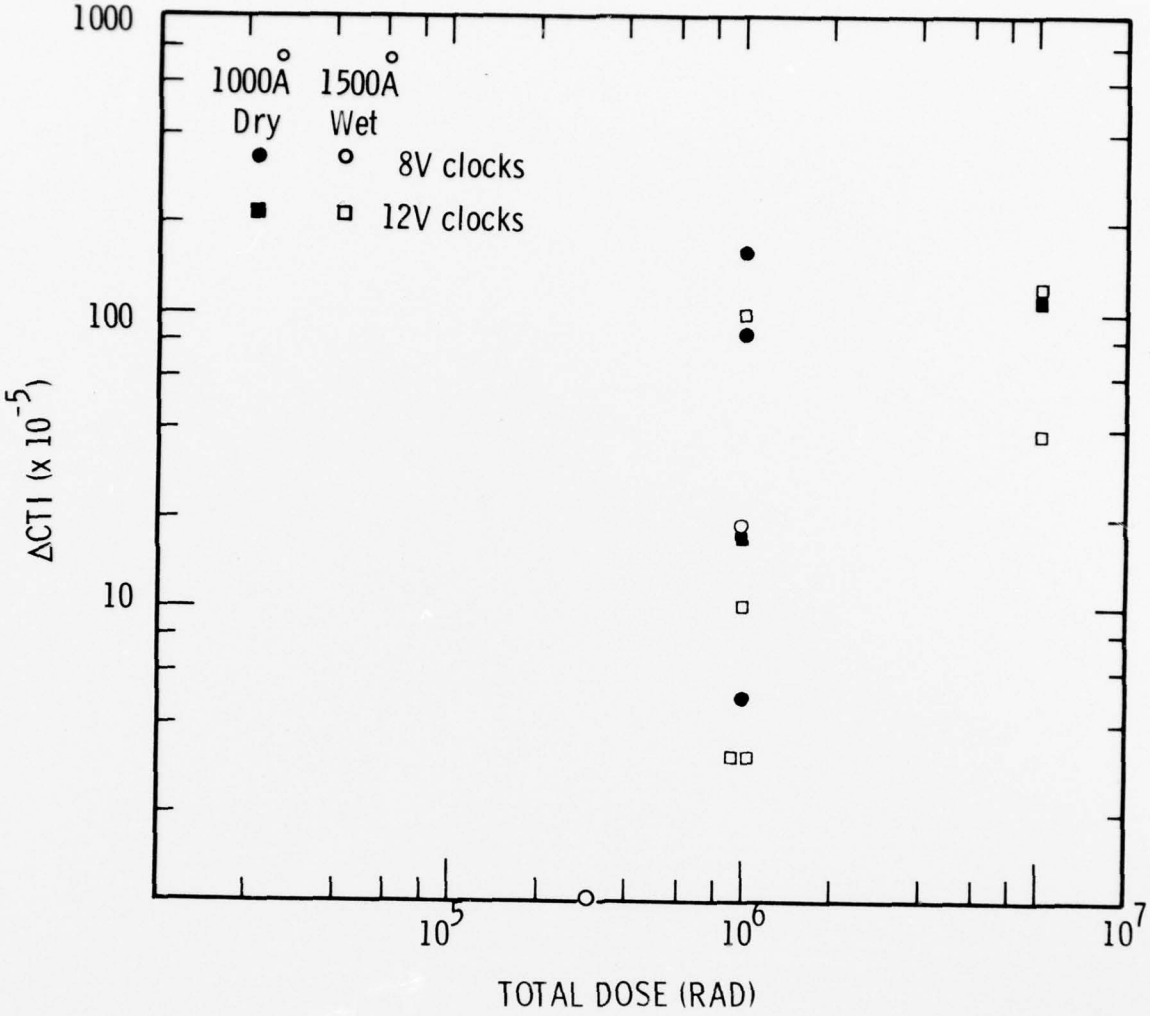


Figure 8 Change in Charge Transfer Inefficiency (CTI) with Gamma Dose

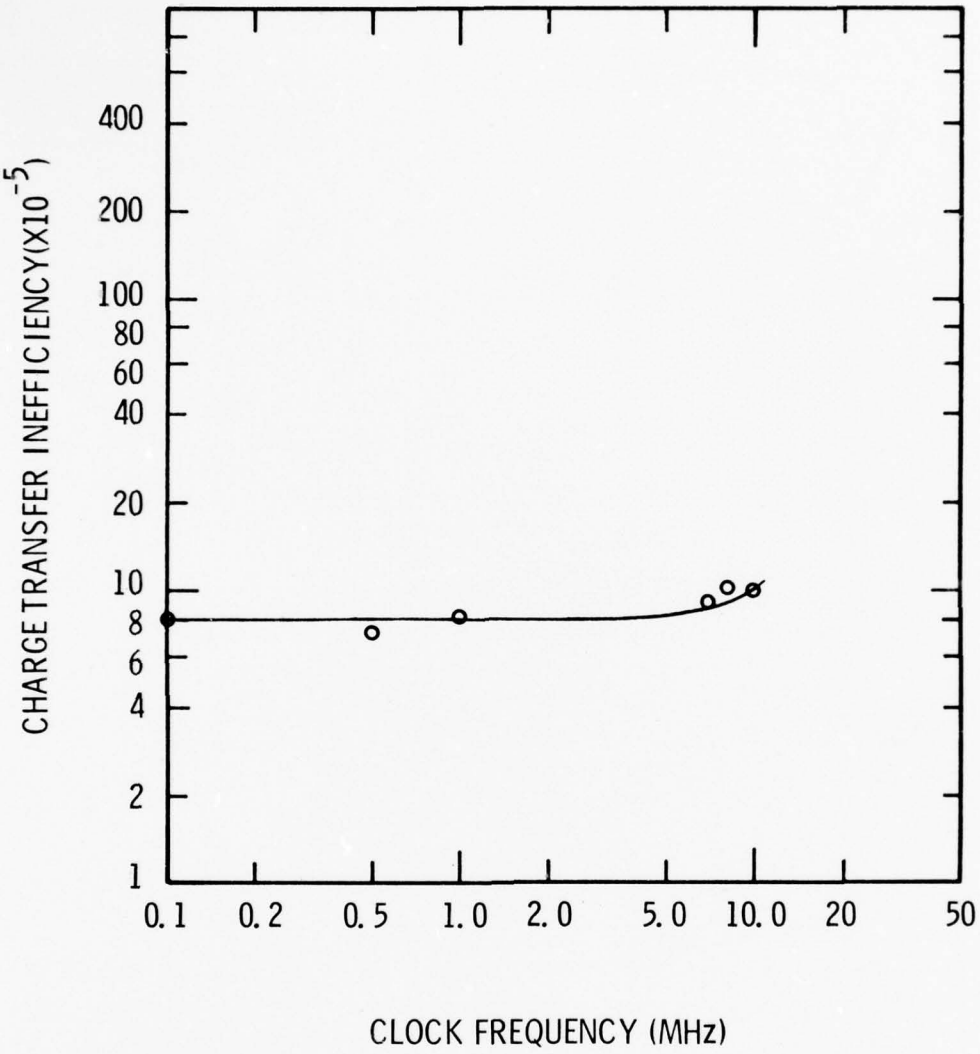


Figure 9 Plot of Charge Transfer Inefficiency Versus Frequency After Co^{60} Dose of 10^6 Rad - Sample 68-4-157

changes for the CCD electrodes due to the different bias conditions on the devices during exposure. The CCD input and output diodes were biased to +24 volts so that the buried layer in the channel could be depleted of electrons. This results in a layer of fixed positive charge, which causes the potential in channel bulk to be higher than the maximum gate voltage. This creates a negative electric field in the gate oxide so that holes or positive ions in the oxide that become mobile during irradiation tend to drift to the gate electrode surface where they have less effect on threshold voltage. However, the test MOSFET diffusions were at zero potential, so the buried layer under the gate could not be depleted since the minimum gate voltage was also zero volts. (A negative gate and substrate bias of 10 to 12 volts is typically required to completely deplete through the buried layer.) The gate bias on the test MOSFET was a square wave of 0 to +12 volts, while on the source-follower the gate was at a dc level of +24 volts. Therefore, these two devices had a large positive electric field in the oxide during irradiation which resulted in much larger threshold shifts and gain degradation.

Because of these bias differences, the threshold voltage shifts measured on the test transistors are not directly applicable to the conditions under the CCD gates or the output source-follower as it is normally biased. They are useful, however, since they show what can be expected for a case where a grounded source MOSFET might be used as in an on-chip clock driver or more elaborate output circuit.

In heavily implanted depletion mode devices such as these it was found that two different threshold voltages can be measured if a significant number of charge trapping states exist at the oxide-silicon interface. One is the pulse threshold, which is dependent on fixed interface charge, and the other is the steady-state or dc threshold, which depends on both the fixed and

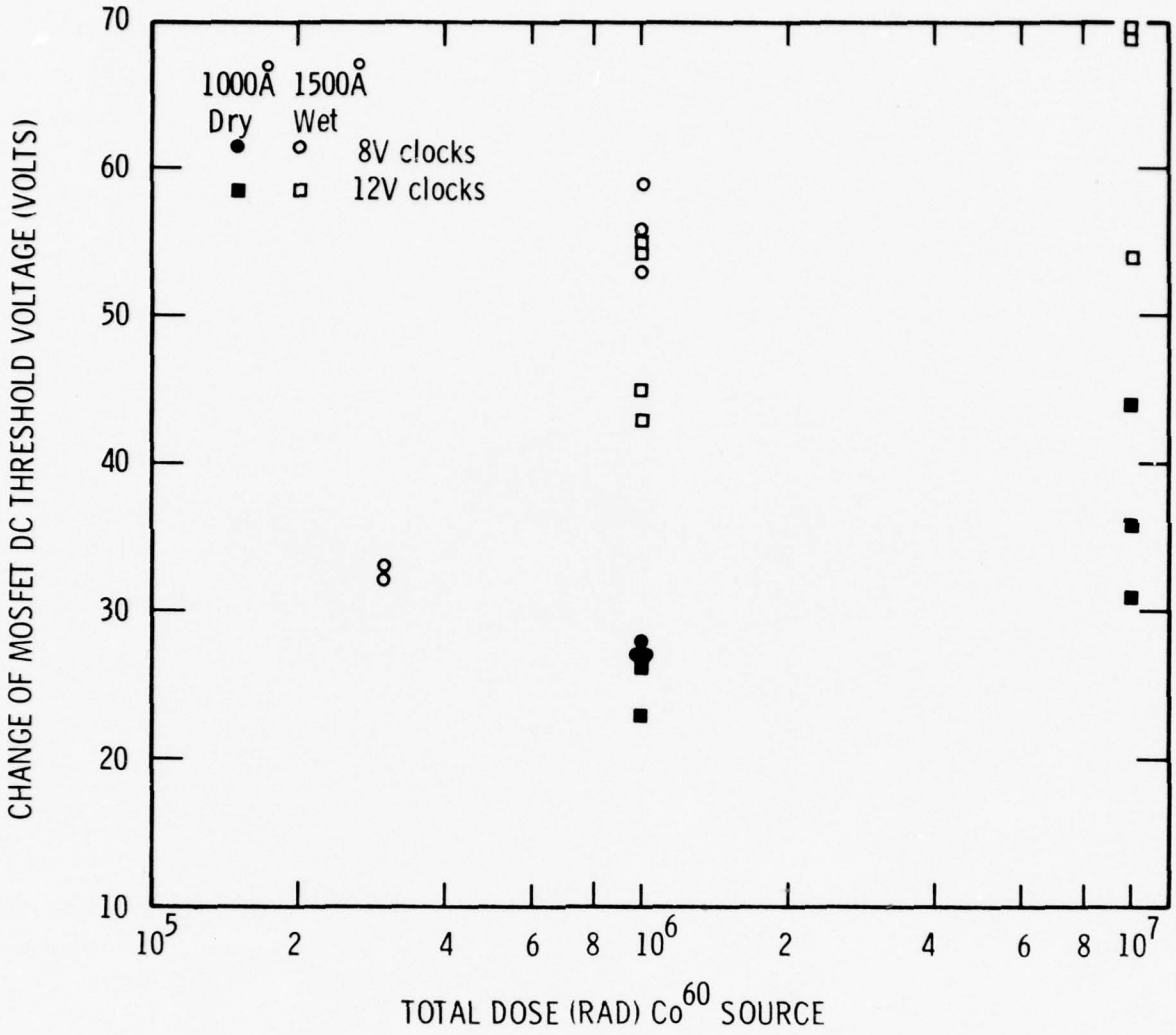
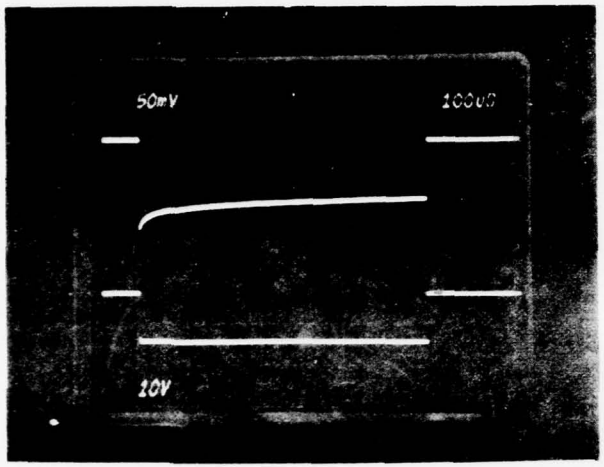


Figure 10 MOSFET Dc Threshold Voltage Shift Versus Total Gamma Dose

trapping state charge. The separate contributions of these two kinds of charge to the threshold voltage can be determined by applying a negative-going step voltage to the gate while observing the source-drain current. If the gate of the MOSFET is pulsed from near zero volts with a negative pulse V_T (pulse) just large enough to overcome the potential due to the fixed charge layer, the source-drain current will be momentarily cut off, but will then again start to flow if there were a significant number of filled trapping states that could empty electrons into the channel. This effect is seen in current waveforms of Figure 11 where it can be seen that the drain current initially went to zero and then increased with time to a new steady-state value as interface states emptied. The size of the negative gate pulse must be increased by an amount $\Delta V_T(ss)$ to keep the channel turned off after the traps empty, and the total number of surface state traps involved is equal to $\Delta V_T(ss) \cdot C_{ox}/q$, where C_{ox} is the gate oxide capacitance. The increase in fixed oxide charge is $\Delta Q_{ss} = \Delta V_T(pulse) \cdot C_{ox}/q$, where $\Delta V_T(pulse)$ is the change in the pulsed threshold voltage after exposure. Figures 12 and 13, which are plots of the test MOSFET threshold voltage shifts due to fixed charge and trapping states versus radiation dose, show that the V_T shifts due to each of these causes were significantly lower for the devices with 1000 Å dry oxide than for the devices with 1500 Å wet oxide. However, there is no significant difference in the total charge buildup, as can be seen in Figures 14 and 15. The difference in thickness between the two oxide types accounts for the difference in threshold voltage, which is inversely proportional to the oxide capacitance and hence its thickness.

The threshold voltage under the CCD electrodes was measured after irradiation by operating the whole CCD as a MOSFET with input and output diodes as source and drain. Threshold measurements were made with all gates connected together and also for the input and output gates individually with all other gates biased on. These measurements were not made before irradiation, so the



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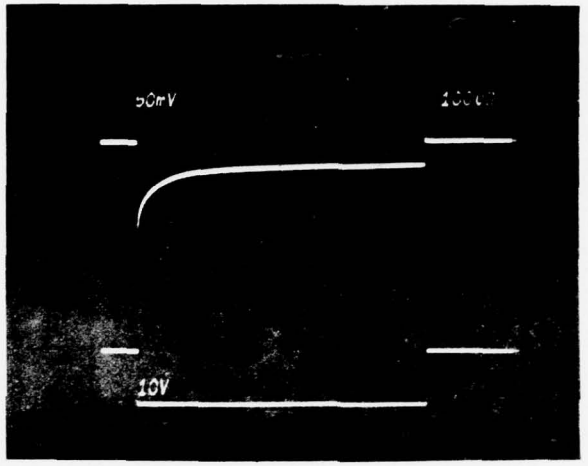


Sample 68-4-157

Variation of MOSFET Drain Current with Time Due to Emptying of Surface State Traps. Top Trace - I_D (2 ma/div), Lower Trace - V_G (10 V/div).

Figure 11 Variation of MOSFET Drain Current with Time

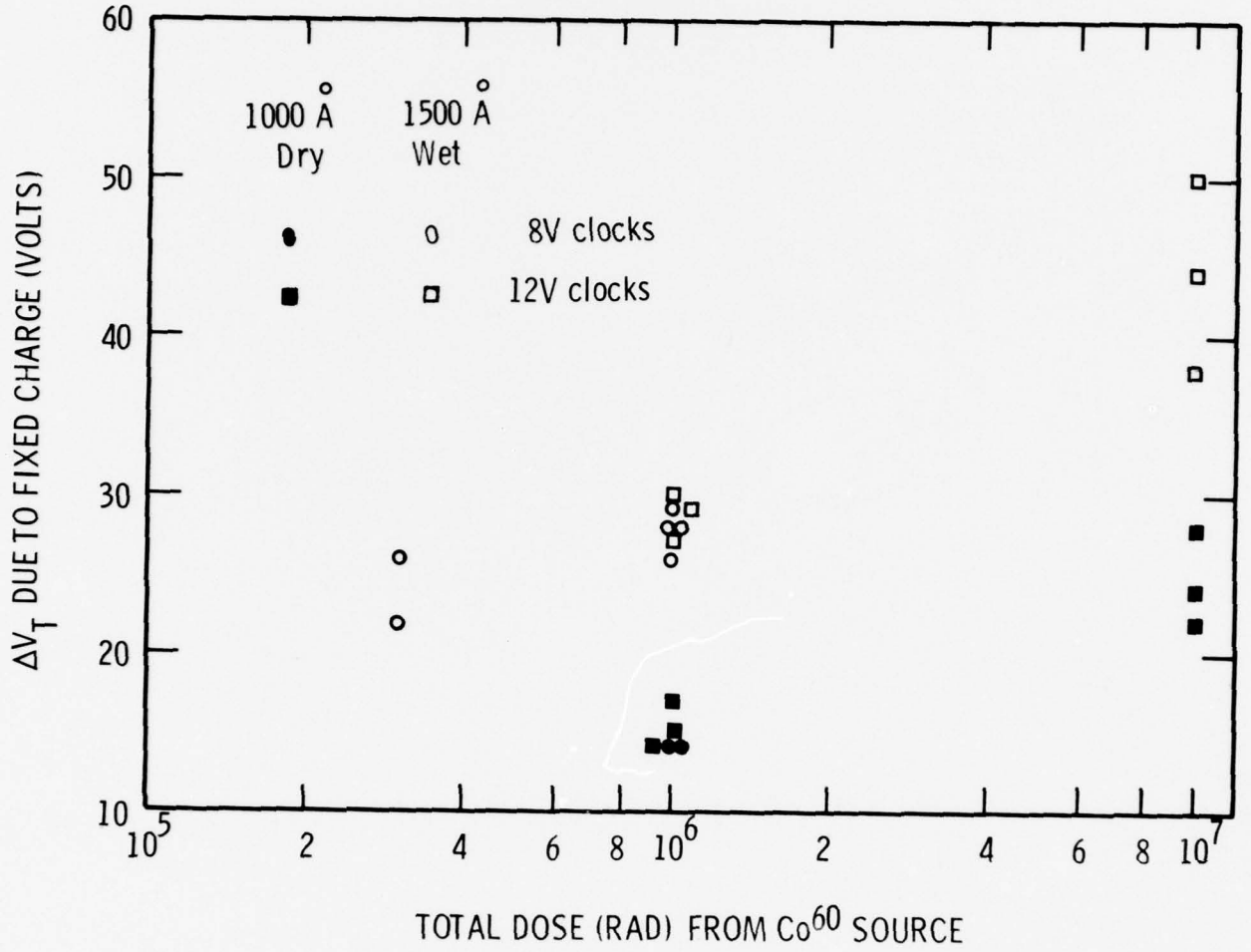


Figure 12 MOSFET Threshold Shift Due to Fixed Charge Increase

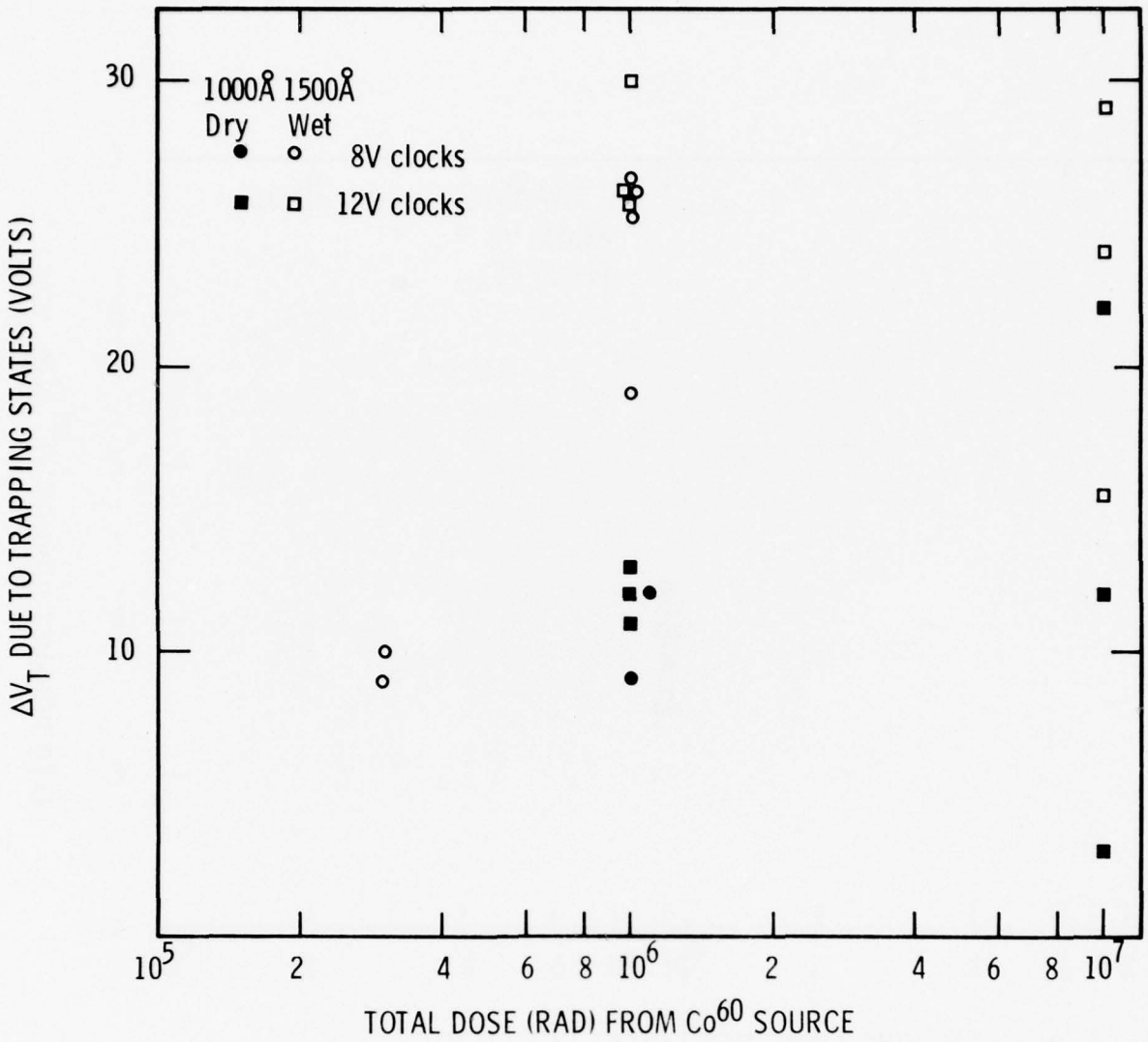


Figure 13 MOSFET Threshold Shift Due to Trapping States

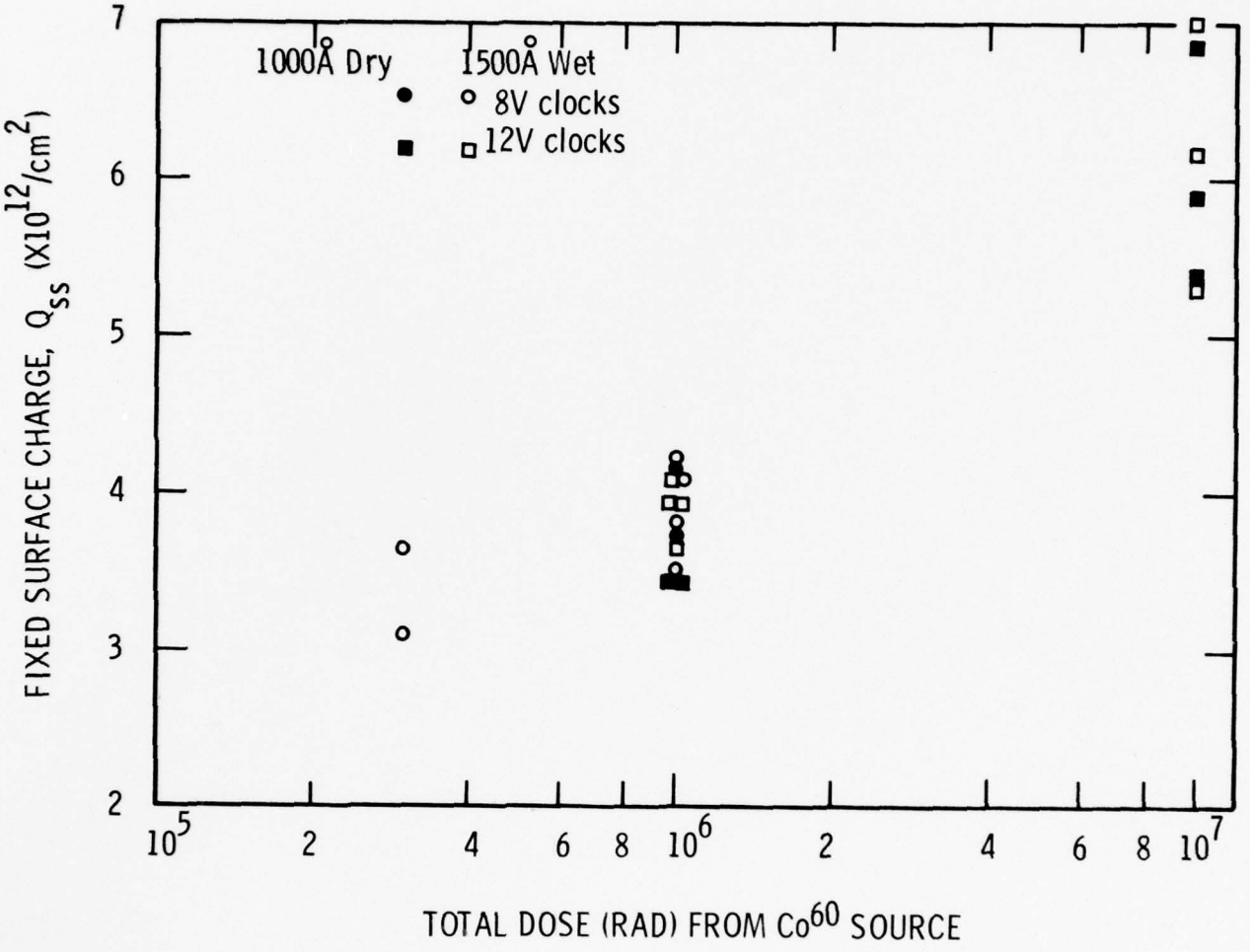


Figure 14 Fixed Charge Increase Versus Gamma Dose

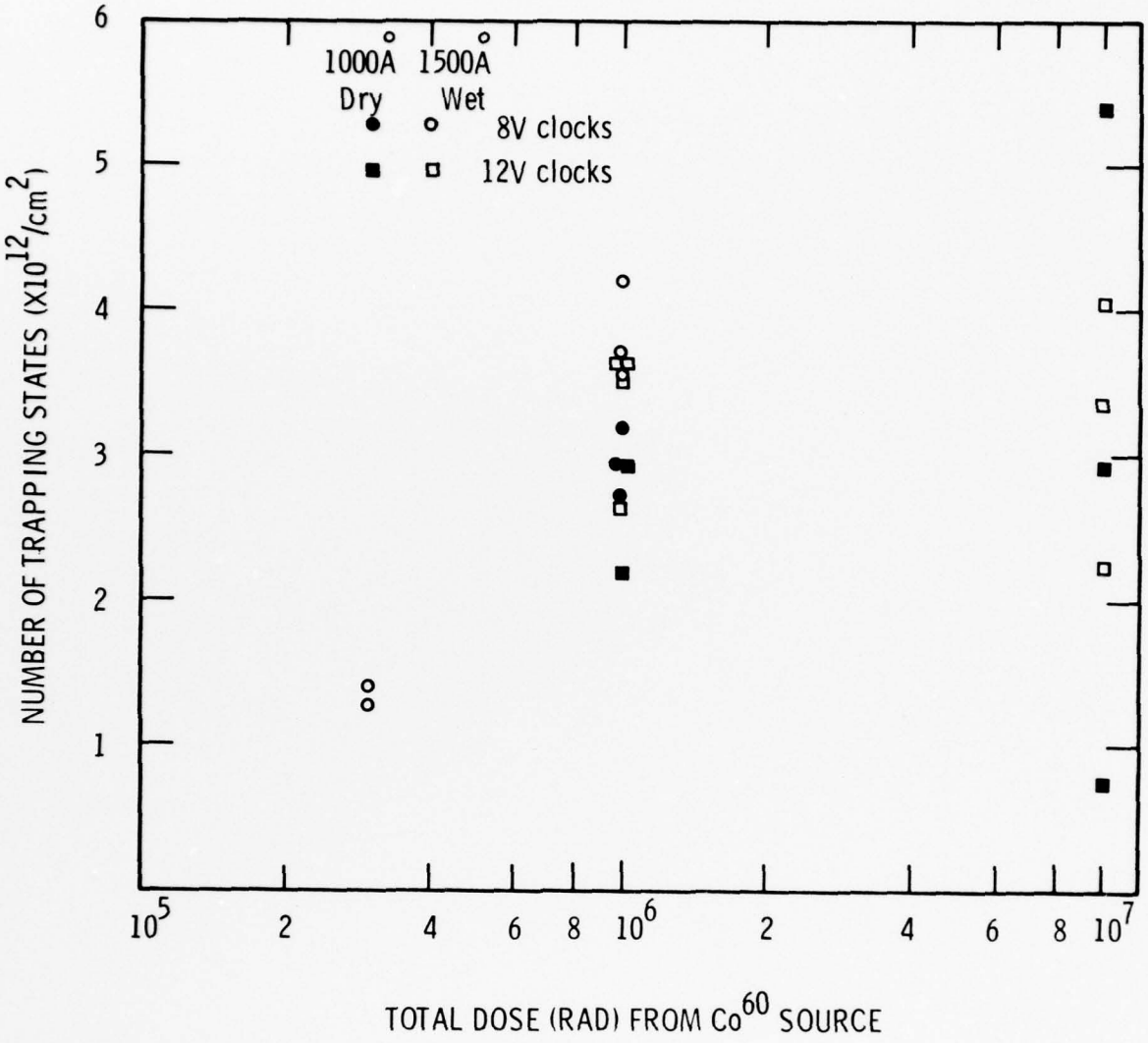


Figure 15 Number of Trapping States Versus Gamma Dose

actual threshold shift for each sample could not be determined. However, based on measurements of nonirradiated devices from the same lot, the fixed charge portion of the V_T shifts ranged from 1 to 2 volts. The trapping state portion that was less than 0.1 volt for nonirradiated devices ranged from less than 0.1 to 1.2 volts after exposure. The corresponding increases in fixed interface charges and total trapping state charge are each less than 3×10^{11} per cm^2. This is an order of magnitude lower than the values seen on the test MOSFETs.

3. Source-Follower Gain

Even though gain degradation in the output source-follower was one of the most severe problems with the Co^{60} gamma-irradiated buried channel devices in this test, it is not expected to be a major problem for devices irradiated under normal operation, provided the operating conditions are chosen such that the gate-to-source voltage is negative. This will keep a negative electric field in the gate oxide and should result in V_T shifts and surface trap increases similar to those seen for the buried channel CCD gates. However, for ion-implanted MOSFETs irradiated with large positive gate-to-source voltages such as the source-follower MOSFETs in this test, large decreases in gain occur, as shown by Figure 16. The pre-irradiation values were from 0.6 to 0.7 for the bias conditions used. Measurement of the variation of the MOSFET transconductance G_m revealed a frequency dependence at certain negative gate biases. This is illustrated by Figure 17, which shows drain current waveforms for a 2 volt ac squarewave gate voltage at several different negative gate bias levels. At a bias level such that the ac signal swing changed the channel surface from accumulation to depletion, the low frequency G_m is reduced by a factor of more than two due to interface state trapping effects. Because of the larger threshold shifts the 1500 Å wet oxide devices were operating near the level of minimum G_m and consequently exhibited low source-follower gain. Very little gain loss occurred for the Linac-irradiated devices because of the different source and drain biases in these tests and because the large photocurrents generated during the electron pulse discharged the output diode and hence the source-follower gate to nearly zero.

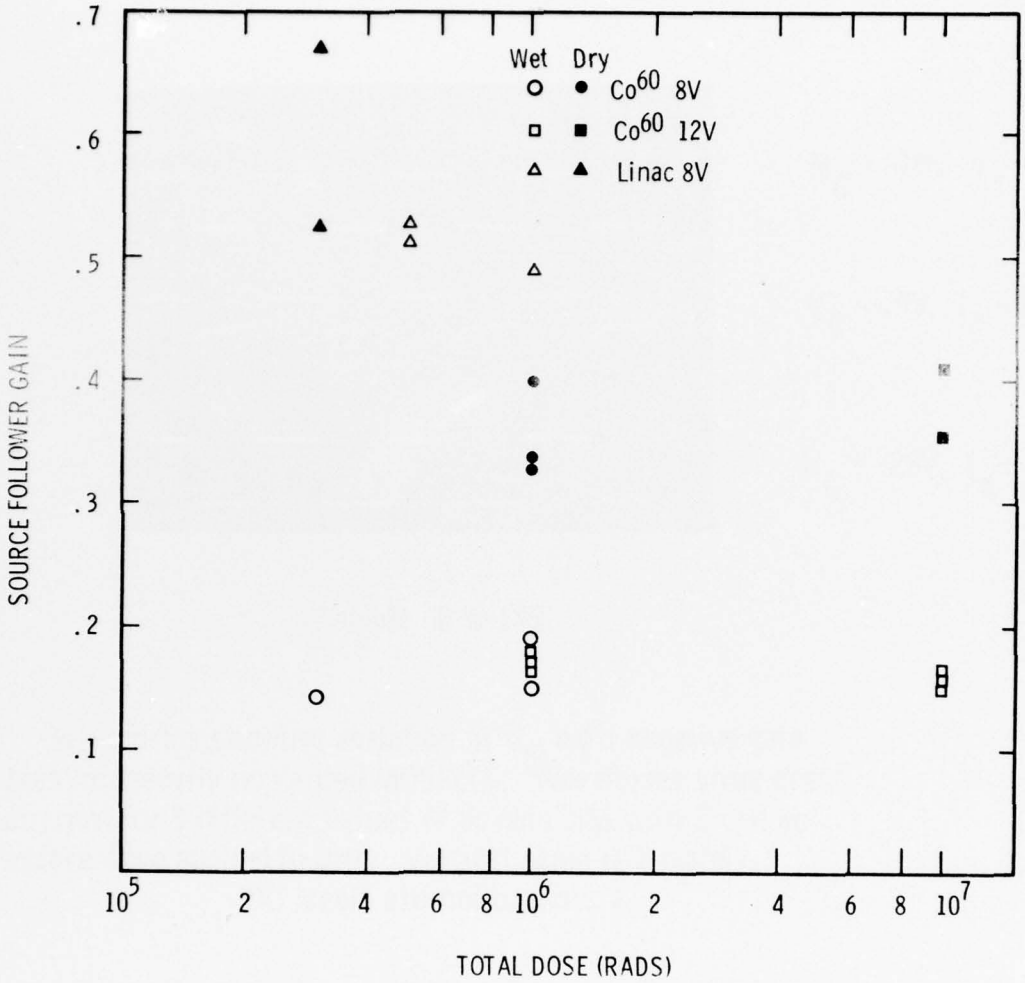
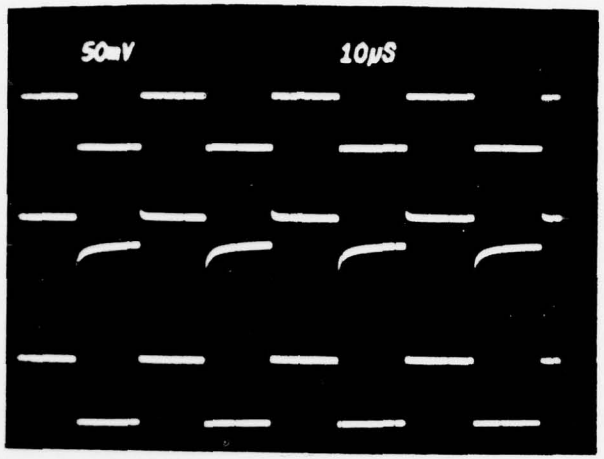


Figure 16 CCD Output Source-Follower Gain Versus Dose



V_G = -10V, I_d = 5.9 ma

V_G = -19V, I_d = 2.6 ma

V_G = -28V, I_d = 1.0 ma

Sample 68-6-145

Waveforms showing variation of G_m with negative gate bias for heavily implanted MOSFETS. Waveforms show drain current for 3 different values of dc gate bias with 2 volt ac square wave applied to gate. Vertical scale is 1 ma/div. (DC levels are not to scale.)

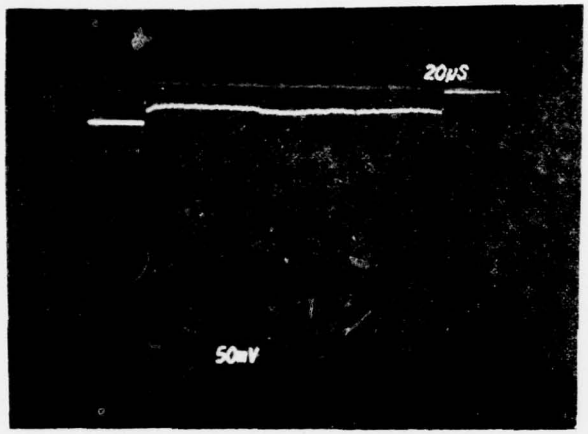
Figure 17 Variation of MOSFET G_m with Negative Gate Bias

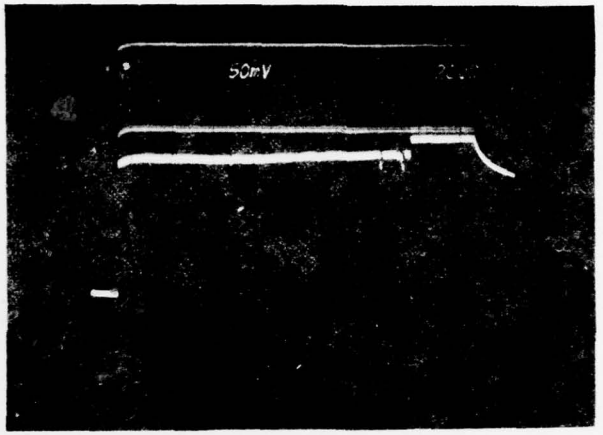
4. Full Well Capacity

The full well charge capacity of the CCDs was determined from the output diode reset current to eliminate the effects of variation of output mode capacitance and source-follower gain. The value of full well capacity varies somewhat with substrate bias and output gate voltage both before and after irradiation, but for similar conditions, the full well capacity was found to be within 20% of initial values. The reduced output signal voltage after irradiation is due almost entirely to the reduced source-follower gain.

5. Leakage Current

Waveforms of the output voltage due to integrated leakage current for a typical sample are shown in Figure 18. Note that although the output voltage level is about the same for both waveforms, the integration time was reduced from 50 msec to 1 msec for the measurement after irradiation. This, plus the reduced voltage gain of the output circuit, caused the voltage to be the same even though the leakage current had increased greatly. The clock voltage for the measurement after irradiation was reduced to 8 volts because the leakage increased nonuniformly near the center of the CCD for higher clock voltages. The gated diode leakage versus gate voltage characteristic for this test sample was examined to determine the cause of the large increase in leakage. It is seen (Figure 19) that leakage from the n^+ diffusion was still low, about 7.5 nA/cm^2. As the gate voltage was increased to the level at which the area under the gate turned on, the leakage increased greatly to about 900 nA/cm^2, and for slightly higher gate voltages it again began a very rapid increase. This type of leakage characteristic indicates a breakdown occurring at the channel stop junction, so the CCD leakage was remeasured with a positive bias on the substrate to reduce the voltage difference between the channel and channel stop. As shown in Figure 20, this reduces the leakage current to about 480 nA/cm^2 and permits clock voltages of up to 10 volts to be used for this particular





Before Irradiation
Integration Time = 50 msec
V_{CK} = 15 V; V_{SUB} = 0 V
J_L = 5.5 nA/cm^2

After Co^{60} Dose of 10^6 Rad
Integration Time = 1 msec
V_{CK} = 8 V; V_{SUB} = 0 V
J_L = 1930 nA/cm^2

Figure 18 CCD Integrated Leakage Current

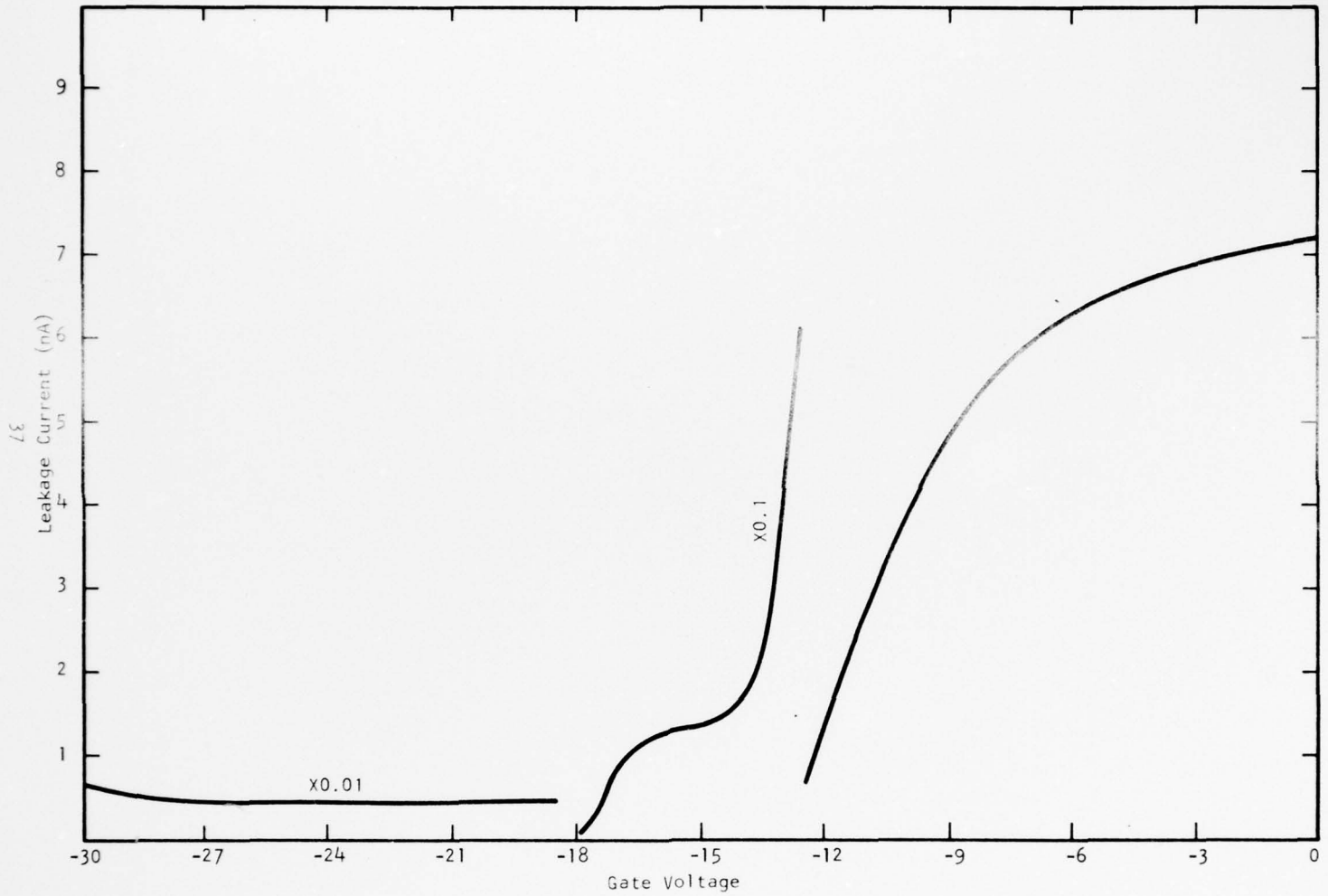
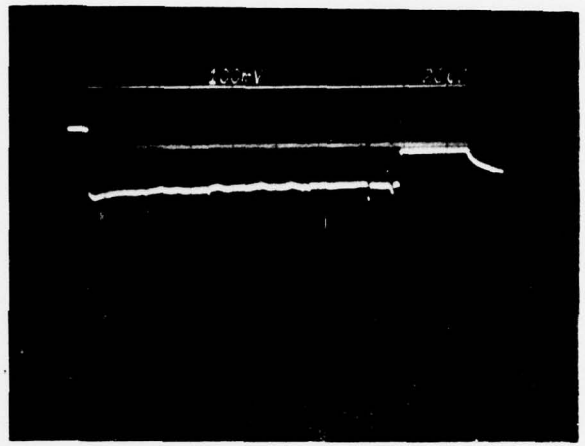


Figure 19 Gated Diode Leakage Current after Dose of 10^6 Rad



After Co^{60} Dose of 10^6 Rad
Integration Time = 5 msec
V_{CK} = 10 V; V_{SUB} = + 10 V
J_L = 480 nA/cm^2

Figure 20 CCD Integrated Leakage Current with Positive Substrate Bias

sample. There were wide variations in leakage after irradiation, as seen in Tables II and III, which list several different parameters for all the test samples. Samples from slice 6 had consistently low leakage currents. This slice had 1000 °C dry gate oxide with thermally deposited metal.

6. Noise

The CCD output noise measurements are listed in Tables II and III. Both pre- and post-irradiation measurements were made at a clock frequency of 200 kHz with band-limiting at slightly higher frequency to prevent wideband noise from the source-follower MOSFET from being aliased by the correlated clamp and sampling process used to remove kTC noise. The pre-irradiation values ranged from 125 to 315 electrons. Subsequent measurements on devices from the same lot disclosed that the bandwidth of the thermal noise from the preset MOSFET during its off state is apparently larger than expected and is large enough so that the correlated clamp and sample process was leaving a significant portion of the kTC noise. By going to a higher clock rate and roll-off frequency, the period between the output clamping and sampling could be shortened. This reduced the amount of kTC noise, and values as low as 75 electrons were measured for nonirradiated devices from the same lot as the test samples. After exposure, typical measured values were from 200 to 800 electrons. Shot noise on the leakage currents of from 1.0 to 6.0 nA ($\approx$ 200 to 1000 nA/cm^2) would be from 190 to 425 electrons, which implies that there is a significant noise source in addition to the leakage current. The most likely source is the output source-follower which has interface state densities of $> 10^{12}/cm^2$ as discussed earlier.

TABLE II

TABULATION OF CHARACTERIZATION DATA FOR TOTAL DOSE TEST SAMPLES ARRANGED BY TEST

o Total Dose 1.2 MeV Gamma Test Samples

Sample No.	Dose (Rad)	Clock Voltage	CTI ($\times 10^{-5}$) Pre	CTI ($\times 10^{-5}$) Post	J_L nA/cm^2 Pre	J_L nA/cm^2 Post	Noise (Electrons) Pre	Noise (Electrons) Post	V_T (MOSFET) Pre	V_T (MOSFET) Post
68-1-76	10^6	12	13	110	5.5	930	315	1700	-12.6	-66
68-3-156	10^6	12	4	14	5.0	690	200	-	-11.0	-56
68-4-157	10^6	12	4	7	5.5	485	170	460	-11.5	-66
68-6-66	10^6	12	3	20	3.7	180	180	480	-10.2	-33
68-8-187	10^6	12	5	-	37	-	300	-	-10.5	-36
68-9-68	10^6	12	4	7	7.4	320	175	-	-11.4	-66
68-1-185	10^7	12	30	-	-	-	230	-	-10.5	-55
68-3-184	10^7	12	5	-	13	905	190	810	-11.3	-75
68-4-167	10^7	12	2	120	9.2	1970	185	-	-11.8	-85
68-6-63	10^7	12	7	120	6.0	160	140	-	-10.7	-42
68-8-59	10^7	12	50	-	-	>2000	-	-	-12.0	-48
68-9-146	10^7	12	2	40	6.5	970	200	210	-13.1	-67
68-3-106	3×10^5	8	4	5	-	415	205	-	-11.5	-44
68-4-106	3×10^5	8	4	-	-	-	-	-	-11.0	-44
68-1-74	10^6	8	9	14	26	440	165	-	-10.9	-38
68-3-134	10^6	8	4	-	-	-	185	-	-11.5	-65
68-4-164	10^6	8	2	20	9.0	510	185	-	-10.8	-64
68-6-145	10^6	8	5	90	3.7	130	125	90	-10.0	-38
68-8-65	10^6	8	40	200	15	310	195	260	-10.0	-37
68-9-129	10^6	8	7	-	-	-	-	-	-11.4	-70

TABLE III

TABULATION OF CHARACTERIZATION DATA FOR TOTAL DOSE SAMPLES ARRANGED BY PROCESS VARIATION

Total Dose 1.2 MeV Gamma Test Samples

Sample No.	Dose (Rad)	Clock Voltage	CTI ($\times 10^{-5}$)		J_L nA/cm^2		Noise (Electrons)		V_T (MOSFET)	
			Pre	Post	Pre	Post	Pre	Post	Pre	Post
68-1-74	10^6	8	9	14	440	-	165	-	-10.9	-38
68-1-76	10^6	12	13	110	5.5	930	315	1700	-12.6	-66
68-1-185	10^7	12	30	-	-	-	230	-	-10.5	-55
68-3-106	3×10^5	8	4	5	-	415	205	-	-11.5	-44
68-3-134	10^6	8	4	-	-	-	185	-	-11.5	-65
68-3-156	10^6	12	4	14	5.0	690	200	-	-11.0	-56
68-3-184	10^7	12	5	-	13.0	905	190	810	-11.3	-75
68-4-106	3×10^5	8	4	-	-	-	-	-	-11.0	-44
68-4-164	10^6	8	2	20	9.0	510	185	-	-10.8	-64
68-4-157	10^6	12	4	7	5.5	485	170	460	-11.5	-66
68-4-167	10^7	12	2	120	9.2	1970	185	-	-11.8	-85
68-6-145	10^6	8	5	90	3.7	130	125	90	-10.0	-38
68-6-66	10^6	12	3	20	3.7	180	180	480	-10.2	-33
68-6-63	10^7	12	7	120	6.0	160	140	-	-10.7	-42
68-8-65	10^6	8	40	200	15	310	195	290	-10.0	-39
68-8-187	10^6	12	5	-	37	-	300	-	-10.5	-36
68-8-59	10^7	12	50	-	-	>2000	-	-	-12.0	-48
68-9-129	10^6	8	7	-	-	-	-	-	-11.4	-70
68-9-68	10^6	12	4	7	7.4	320	175	-	-11.4	-66
68-9-146	10^7	12	2	40	6.5	970	200	210	-13.1	-67

SECTION VII

LINAC TOTAL DOSE TESTS

Total dose effects tests were made using 100 nsec wide, 20 MeV electron pulses of about 80 rad per pulse and 10 pulses per second. The source was turned off, and data were taken at levels of 0, 5×10^4, 10^5, 3×10^5, and 10^6 rad unless the device failed or degraded to the extent that useful data could not be obtained at a lower level. The CCD input threshold was found to shift by 3 to 6 volts at 10^6 rad, depending on oxide thickness, for the input method used, which was to apply the signal to the input diode. This input threshold shift can be eliminated by using the technique of introducing the signal on the input gate as described in Appendix B of Interim Technical Report No. 1 for this contract. Typically, one-half of this shift occurred by a dose level of 10^5 rad, and little shift was seen after 5×10^5 rad, as seen in Figure 21. The CCDs typically had a large increase in leakage current at about 3×10^5, which made further CTI measurements difficult. It was later found that the leakage current could be reduced by going to a positive substrate bias as in the Co^{60} irradiated samples.

One very different result for these tests was that the source-follower gain was degraded much less than was the case for the Co^{60} tests. This is due to the fact that for a high dose rate source, the CCD output node is discharged to nearly substrate voltage by the large photocurrent during the radiation. Therefore, the gate bias on the source-follower is nearly zero during irradiation compared to a gate bias of about +24 volts for buried channel devices in the low dose rate Co^{60} tests. The V_T shifts measured for the CCD gates on the samples were on the order of 2 volts.

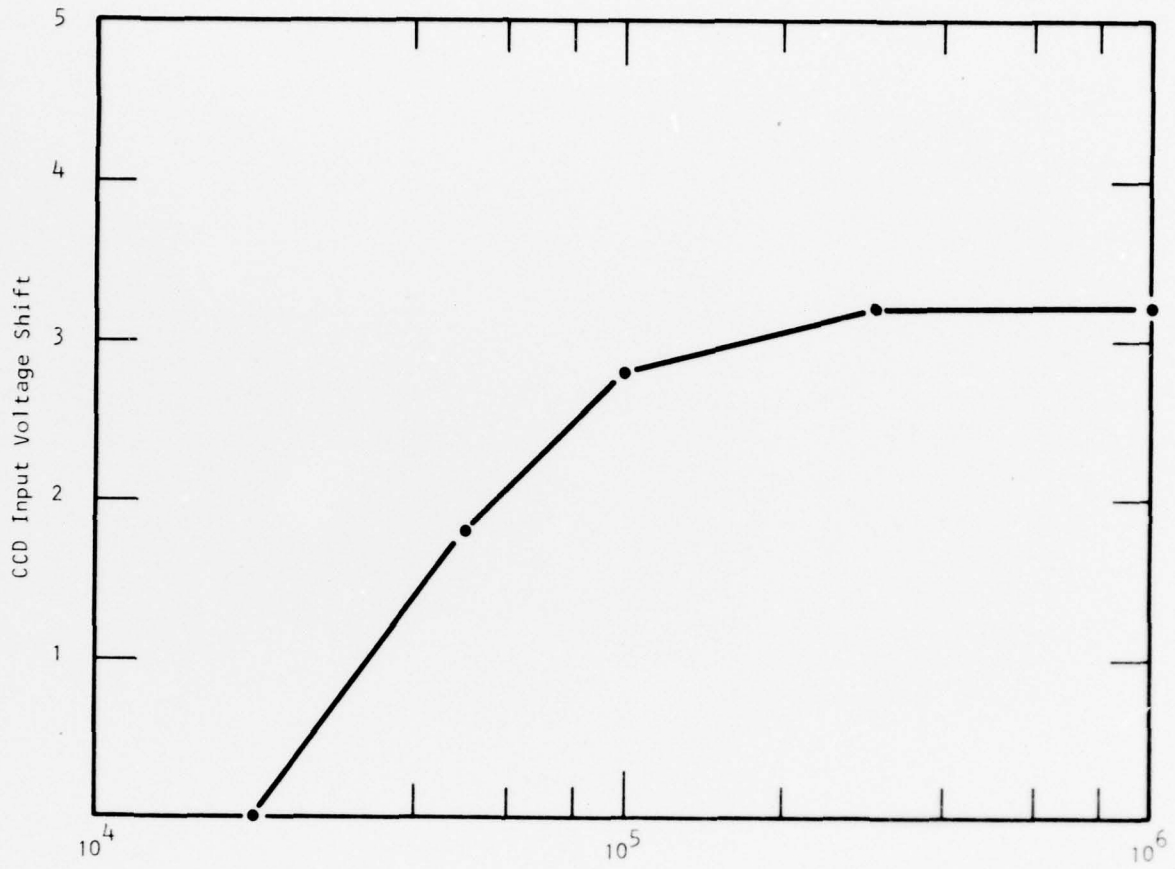


Figure 21 Input Threshold Shift Versus Dose for Linac Total Dose Tests (Sample 68-6-175)

SECTION VIII

CONCLUSIONS

The second group of tests has shown that it is possible to maintain charge transfer efficiency as high as 0.9999 after a gamma dose of 10^6 rad for some samples of the buried channel, double-level aluminum gate CCDs tested, although other samples had larger CTE degradation. The most serious degradation caused by the gamma radiation from Co^{60} is the increase in leakage current. Further understanding of the exact mechanism of this leakage is needed so that device processing and operating conditions can be modified to minimize it. The large V_T shifts and bias-dependent gain degradation seen in the MOSFET test devices is due to the bias conditions used during exposure, which were much worse for radiation damage than the normal source-follower operating bias. Gain loss and V_T shifts should not be a major problem for MOSFETs that are operated in the buried channel mode, but will be for buried channel devices of the type tested if operated with the surface conducting.

The threshold voltage shift has been found to be very dependent on oxide field. Threshold shifts at 10^6 rad vary from less than 2 volts for a negative oxide field to greater than 50 volts for large positive oxide fields. No definite conclusions have been reached regarding the relative hardness of steam versus dry oxide. Any possible advantages of the low temperature dry oxide growth may have been negated by the ion-implantation through the gate oxide. It can be seen from these results that thinner gate oxides result in less V_T shift for a given amount of charge buildup and thus appear harder.

The dose rate tests described show that the devices tested will recover from bursts of ionizing radiation at levels $> 10^{10}$ rad/sec in a period of less than 300 μsec when clocked at 1 MHz and suffer no permanent damage. Without external current-limiting, permanent thermal damage begins to occur at dose rates of 4×10^{10} rad/sec for 100 nsec pulses.